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Resistive Switching of Spinel $Li_4Ti_5O_{12}$ Lithium-Ion Battery Material for Neuromorphic Computing

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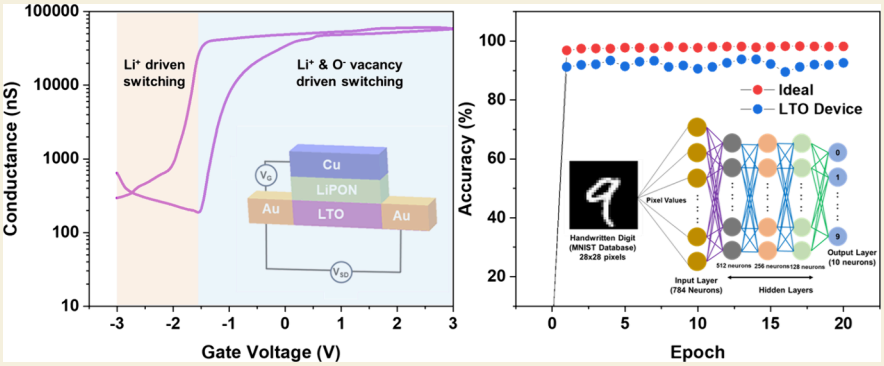

ABSTRACT: The rapid rise of AI has exposed significant limitations in conventional Von Neumann computing architecture, particularly in regard to speed and energy efficiency. To address these challenges, researchers are exploring a brain-inspired neuromorphic architecture that mimics biological neural networks, enabling massive parallel processing with reduced power consumption for complex AI computational demands. Recent interest has focused on utilizing battery electrodes and solid electrolyte materials for their resistive switching properties in developing a neuromorphic architecture. These properties are precisely tuned through local- and bulk-level chemical composition modifications via voltage bias stimuli. In this study, we demonstrate fabricating a three-terminal lithium-ion electrochemical transistor based on lithium titanium oxide ($Li_4Ti_5O_{12}$), a popular lithium-ion battery anode material. We deposited and characterized LTO thin films using RF sputtering, demonstrating a 6 orders of magnitude increase in electronic conductivity upon lithiation, with conductivity plateauing after 20% lithiation. Density functional theory calculations revealed transformation from the insulating to conducting state, supported by experimental characterization through X-Ray Photoelectron Spectroscopy (XPS) and Direct Current (DC) polarization analyses. The fabricated transistor consisted of LTO as the channel layer, gold as source/drain terminals, lithium phosphorus oxynitride (LiPON) as the lithium-ion conductor, and copper as the gate terminal. The device exhibited clear hysteresis in transfer characteristics due to lithium insertion/extraction processes. Long-term potentiation (LTP) and long-term depression (LTD) measurements showed an asymmetric ratio of 1.425 and maximum/minimum conductance ratio of 7.83. When implemented in a deep neural network (DNN) for MNIST handwritten digit recognition, the device achieved 92.03% accuracy over 20 training epochs. Detailed transport mechanism analysis revealed the crucial role of oxygen vacancies and interface effects in device operation. Our preliminary findings establish LTO-based lithium-ion electrochemical transistors as promising candidates for energy-efficient neuromorphic computing applications, offering potential solutions to traditional Von Neumann architecture limitations.

KEYWORDS: *$Li_4Ti_5O_{12}$, Li-Ion Gated Transistor, Li-ion Battery, Thin Film, Resistive Switching, LiPON, Neuromorphic Computing*

INTRODUCTION

The growth of artificial intelligence (AI) in computing and data processing has been staggering in the past several years. The processing hardware required to run these AI algorithms is the major limitation of this growth, as it is constrained by speed and energy efficiency.[1,2] The main reason for this limitation is the widely used Von Neumann architecture for processing

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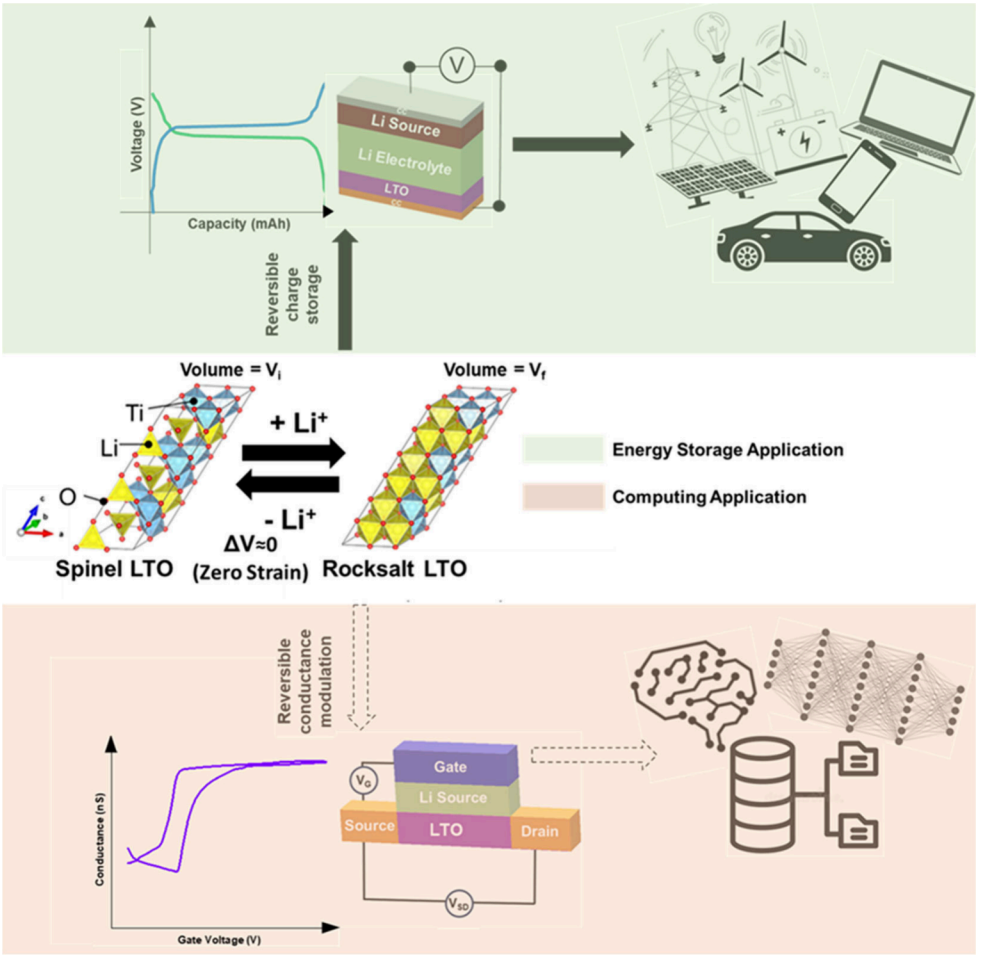

Figure 1. Versatility of LTO's lithium (de)intercalation for energy storage and computing applications.

hardware, which places processing and memory storage in different locations. Therefore, handling data for processing and storing becomes sequential and consumes time and energy. To overcome these challenges of Von Neumann architecture, another type of architecture called neuromorphic architecture is proposed. In this architecture, the processing hardware mimics the functioning of a human brain and facilitates a state-of-the-art computing system different from conventional Von Neumann architecture.[3] To improve energy efficiency and speed, neuromorphic architecture uses embedded crossbar memory arrays that perform parallel operations.[4]

The neuromorphic behavior is achieved through a biological synaptic cleft between two neurons in the human brain. To mimic this behavior for the neuromorphic architecture, various artificial synaptic mechanisms have been proposed, such as filament-forming metal−insulator−metal (MIM) structures,[5−10] phase change memory materials,[11−13] ferroelectric materials,[14−17] and charge-trapping materials,[18−20] to name a few. Our previous work on lithium lanthanum titanium oxide (LLTO),[21] a lithium-ion solid-state electrolyte, showed resistive switching of up to 3 orders of magnitude in a MIM configuration.

Among the various approaches to neuromorphic computing, three-terminal devices have emerged as a promising candidate. Three-terminal devices enhance operational control through dedicated program and read pathways, minimizing interference and enhancing system reliability. This architecture proves particularly valuable for memory systems and neuromorphic computing, where it facilitates precise synaptic weight adjustments while supporting concurrent read/write operations. Currently, several categories of three-terminal devices are being explored for neuromorphic applications. Memtransistors, which combine the functionalities of memristors and transistors, have demonstrated impressive synaptic characteristics. For instance, Sangwan et al.[22] utilized MoS_2 to create world's first memtransistor with multiple programmable states, heterosynaptic plasticity, and low switching energies. More recent work by Leong et al.[23] and Jayachandran et al.[24] has further advanced memtransistor technology, achieving enhanced plasticity, multimode synaptic functionalities, multibit storage capabilities, and lower energies. Another prominent three-terminal approach involves ferroelectric field-effect transistors (FeFETs), as demonstrated by Lederer et al.,[25] which leverage ferroelectric materials' polarization to achieve nonvolatile memory states with fast switching speeds, CMOS compatibility, tunable linearity, and low energy consumption. Electrochemical transistor devices working similarly to lithium-ion batteries, based on lithium-ion intercalation and deintercalation, have recently been gaining attention[26−31] due to their low activation energy for lithium diffusion, lower overpotential, and lower voltage window of operation and biomimetic operation that closely resembles biological synaptic functions—factors that can potentially enable energy efficiency like that of a human brain. Li-ion electrochemical transistors operate via actual ionic transport mechanisms that closely mimic biological neural signaling pathways, offering more authentic neuromorphic

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functionality than the electron−hole-based transport in traditional memtransistors. This fundamental biomimicry enables more direct implementation of synaptic functions through electrochemical doping processes that parallel the ion-channel-mediated signaling in neurons, potentially allowing for more efficient and biologically realistic artificial neural networks despite their relatively slower operational speeds compared to electronic devices.

Among the first studied lithium-ion-based electrochemical transistors, the lithium-ion source and conductor were ionic liquid-based[32−35] or liquid electrolyte-based.[36−38] Even though they possess high lithium-ion conductivities at room temperature, very large-scale integration (VLSI) of these devices on a chip with liquids proved difficult, as they would suffer from device stability, chemical incompatibility, and scaling issues. Therefore, there is a need to develop all-solid-state lithium-ion-based electrochemical transistors. Fuller et al.[28] demonstrated the first all-solid-state lithium-ion-based synaptic transistor (LISTA) using lithium cobalt oxide (LCO) as the channel layer, lithium phosphorus oxynitride (LiPON) as the lithium-ion source, and silicon as the gate terminal. This device exhibited low noise and energy efficiency akin to that of the human brain (based on device simulations). It also demonstrated structural stability, making it scalable for dense crossbar array integration. Nikam et al.[29] showed the importance of higher ionic conductivity of the lithium-ion source on the synaptic functionality of the all-solid-state lithium-ion synaptic transistor by comparing LiPON and lithium phosphorus oxyselenide (LiPOSe) as lithium-ion source with LCO as the channel layer. Most early all-solid-state lithium-ion electrochemical transistors primarily utilized p-doped channel layers like $LiCoO_2$ (LCO), where conductance changes relied on lithium extraction. This mechanism required large negative gate voltages (below −3 V) that could potentially damage the lithium-ion source layer. In contrast, n-doped materials operate through lithium insertion and can achieve conductance modulation at lower gate voltages (≤3 V), offering a more favorable operational range.

Spinel $Li_4Ti_5O_{12}$ (LTO) is a popular lithium-ion battery anode and an n-doped material that can modulate its conductance upon lithium insertion. So far, LTO has been mostly used for reversible charge storage for energy applications.[39,40] However, based on its conductance modulation property, it can be a potential candidate for applications such as neuromorphic computing (Figure 1). In this work, we investigated LTO for resistive switching applications by examining its electronic and ionic transport mechanisms. We demonstrated systematic phase transformation from $Li_4Ti_5O_{12}$ (spinel) to $Li_7Ti_5O_{12}$ (rocksalt) upon electrochemical lithiation, accompanied by a transition from insulating to conducting behavior. Using a three-terminal device architecture with LTO as the channel layer, we achieved resistive switching with synaptic plasticity-like characteristics. When implemented in a deep neural network (DNN) simulation for handwritten digit recognition, the device achieved a 92.03% accuracy. Analysis of the LTO−LiPON interface revealed that the switching mechanism is governed by lithium-ion transport and oxygen vacancy formation, providing insights for neuromorphic computing applications.

EXPERIMENTAL METHODS

Synthesis of the $Li_4Ti_5O_{12}$ Thin Film

The LTO thin film was deposited using radio frequency (RF) sputtering with the help of a commercial $Li_4Ti_5O_{12}$ target-purity of 99.993 wt % (Toshima Manufacturing Co Ltd.). The thin film was deposited on a 1 cm × 1 cm alumina substrate with purity 99.6 wt % (Valley Design Corp) coated on both sides with platinum (Pt) and chromium (Cr). The Cr interlayer was added onto the alumina substrate before Pt was sputtering to improve the adhesion of Pt on the alumina substrate. The Pt−Cr layer was deposited on the opposite side of the LTO thin film to serve as the current collector when the film is lithiated electrochemically. The RF power used in the process was 90 W, and the chamber pressure used was 15 mTorr to initiate plasma so that there was a layer-by-layer growth of the thin film. The lost lithium in the LTO thin films during sputtering was compensated by electrochemically infusing the thin films in a coin cell by using Li metal as the counter electrode. The electrolyte used for the electrochemical infusion process was LP 57 (Gotion Inc.), which is 1 M lithium hexafluorophosphate ($LiPF_6$) in a 3:7 by volume mixture of ethylene carbonate (EC) and ethyl methyl carbonate (EMC). The electrochemically infused LTO film was annealed in a box furnace at a constant temperature of 700 °C for 1 h with a heating ramp rate of 9.5 °C/min to crystallize to the spinel structure.

Out-of-Plane Electrical Conductivity of Pristine LTO, Lithiated LTO Powders, and Thin Films

For the baseline out-of-plane electrical conductivity, LTO pristine powder (Xiamen TOB New Energy Technology Co. LTD) (without conducting agent and binder) was electrochemically lithiated to 4%, 20%, and 100% discharge states in a split cell setup with a Li metal chip/foil as the counter electrode. After lithiation, the powders were washed using dimethyl carbonate (DMC), dried to remove electrolytes and some Solid Electrolyte Interface (SEI) components (if present), and collected for a two-probe direct current (DC) polarization study. The powders collected after drying were again used in the split-cell setup for a two-probe DC polarization study. In the split-cell configuration, approximately 50−75 mg of powder was pressed up to 3 t, and a constant voltage of 0.1 V was applied across the terminal of the split-cell. The stabilized current was noted for the powders for each lithiation. For the out-of-plane electrical conductivity of the thin film, LTO films grown on Pt−Cr coated alumina were electrochemically lithiated to 4%, 20%, and 100% discharge states in a coin cell with a Li metal chip/foil as the counter electrode. The electrolyte used for the lithiation of both thin films and powder was LP 57, which is 1 M $LiPF_6$ in a 3:7 by volume mixture of EC and EMC. After lithiation, the films were washed using DMC, dried to remove electrolyte and SEI components (if present), and placed in the thermal evaporation chamber. In the evaporation chamber, Cu was evaporated to a thickness of 100 nm as the blocking electrode for electrochemical impedance spectroscopy (EIS) and two probe DC polarization measurements. The EIS measurements were performed before DC polarization to rule out any electrical short behavior in thin films due to pin holes. The EIS measurements were performed from 3 MHz to 100 mHz with an applied potential of 10 mV using a Bio-Logic SP-200 at 25 °C. The results were fit using EC-Lab Software. For the two-probe DC polarization study, Pt and Cu were used as blocking electrodes with a constant voltage of 1 V, and the thickness of LTO films was 600 nm−1000 nm to avoid any pin holes. The stabilized current was noted for the LTO films for each lithiation.

Device Fabrication and Testing

The devices were fabricated on a 1 cm × 1 cm alumina substrate. The source and drain terminals were patterned by using UV lithography. The source and drain terminals were made of Au and LTO, and LiPON was deposited using a shadow mask. The LTO was annealed to convert to a spinel structure before LiPON was deposited. The LiPON was deposited using RF sputtering in a pure N_2 environment with a chamber pressure of 12 mTorr and RF power of 50 W using a commercial 2 in. Li_3PO_4 with target-purity 99.9 wt % (Plasmaterials Inc.). After the deposition, devices were transferred to the thermal evaporation

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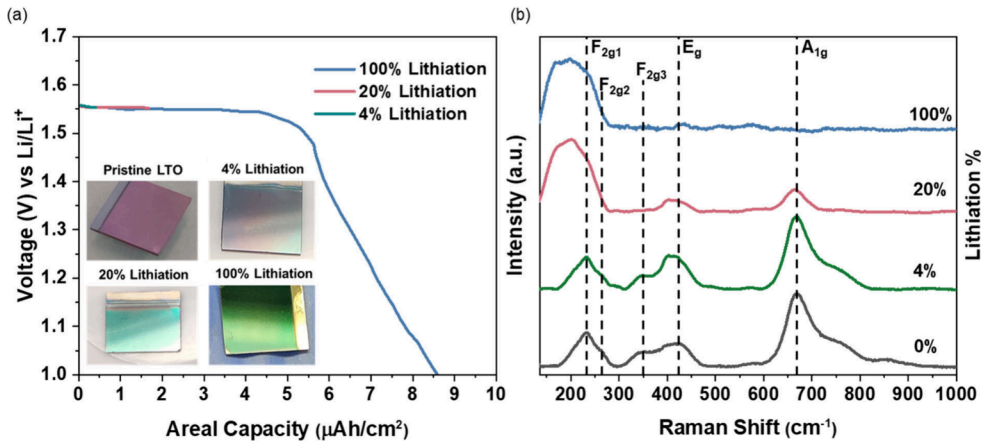

Figure 2. (a) First lithiation profile of LTO thin film for various percentages of lithiation with optical images of washed LTO thin films. (b) Raman spectra of LTO thin films for various percentage lithiation.

chamber to deposit Cu as the gate terminal, with a thickness of 100 nm. Si_3N_4 was deposited using a commercial Si_3N_4 target for Si_3N_4-based devices. The devices were then tested and characterized using an Agilent B1500A semiconductor device analyzer at room temperature in air.

First-Principles Calculation for the Electronic Structure of LTO

The electronic structure of LTO was investigated in the spin polarized GGA+U approximation to density functional theory (DFT). The projector augmented-wave (PAW) method pseudopotentials were employed as implemented in the Vienna Ab initio Simulation Package (VASP). The Perdew−Burke−Ernzerhof (PBE) exchange correlation and a plane-wave representation for the wave function were used, where a cutoff energy was set at 600 eV. The Brillouin zone was sampled with a k-points mesh of $6 \times 6 \times 2$ for density of states (DoS) calculations. The effective U value used through all the calculations was 5 for Ti.

Transmission Electron Microscopy (TEM) and Electron Energy Loss Spectroscopy (EELS)

The TEM analysis was performed on a ThermoFisher Talos X200 equipped with a Gatan Oneview camera operated at 200 kV and UltraFast dual EELS spectrum imaging detector. STEM and EELS were performed on particles extracted from the pristine LTO thin film. EELS spectra presented in this work were acquired from areas without prebeam irradiation to minimize possible electron beam irradiation effects.

Raman Spectroscopy

Raman spectroscopy measurements were performed using a Renishaw inVia Raman microscope. The measurements were run using a 532 nm green laser source with 1800 L mm^{-1} grating and with 20× magnification.

X-ray Photoelectron Spectroscopy (XPS)

XPS was performed with a Kratos AXIS Supra. The samples were rinsed by propylene carbonate (PC) inside an Ar-filled glovebox to remove excess electrolytes and then dried under a vacuum. All samples were loaded in the XPS through an N_2 glovebox with <0.1 ppm water and oxygen without air exposure. The chamber pressure was $<10^{-8}$ Torr during all measurements. XPS spectra were fitted with Casa XPS.

Inductively Coupled Plasma−Mass Spectroscopy (ICP-MS)

ICP-MS analysis was performed using a Thermo iCAP RQ to analyze the elemental concentration of Li and Ti to calculate their ratio to determine the stoichiometry. The samples were digested using concentrated H_2SO_4 and H_2O_2 and heated to ∼210 °C.

Plasma Focused Ion Beam Scanning Electron Microscopy (PFIB-SEM)

PFIB-SEM was performed on a Helios 5 Hydra Dual Beam. A 200 nm thick Pt protection layer was deposited via electron beam evaporation followed by a 1 μm thick Pt layer deposited using ion-beam deposition. The cross section was then milled by using a Xenon plasma ion beam at a 52° tilt with a beam current of 4 nA, followed by a cleaning step with a 53.5° tilt and a reduced beam current of 0.3 nA.

RESULTS AND DISCUSSION

Characteristics of Pristine LTO and Lithiated LTO Thin Films

Conventionally, $Li_4Ti_5O_{12}$ is made into a composite by mixing it with a conducting agent and binder as a lithium-ion battery anode. The presence of a conducting agent and binder strongly influences its electronic and ionic properties. Therefore, to understand the electronic and ionic properties of the pure material for the switching device, we used LTO thin films in this study. LTO was sputtered on a Pt and Cr coated (∼100−200 nm) alumina substrate by using an RF sputtering process. Lithium loss was compensated by electrochemical infusion (Table S1 and Supplementary Note 1), and it was further annealed at 700 °C for 1 h in the ambient atmosphere to obtain the spinel structure (Figure S1 (a)). The surface and cross-section of pristine LTO are shown in Figure S1 (b). The cross-section shows a porous and agglomerated structure after the annealing process. The film was further characterized by HRTEM and STEM-EDS to understand the local structural information on the LTO thin film. For the (111) lattice plane of the LTO, the expected d-spacing value based on the cubic phase is 0.482 nm. From the fast Fourier Transform (FFT) of the HRTEM image, the measured value is 0.488 nm for the obtained LTO thin film, which is in good agreement with the theoretical calculations (Figure S1 (c)). In addition, the STEM-EDS mapping (Figure S1) demonstrates the O/Ti ratio is close to the stoichiometric ratio of 2.4. Furthermore, EELS was performed to compare the oxidation state of Ti in LTO powder as the baseline and LTO thin film. For the Ti L edge, L_2 and L_3 edges split into two t_{2g} peaks at 458 and 464 eV, respectively, and two e_g peaks at 460.5 and 466 eV, respectively, which is consistent with the baseline LTO powder. For the Li K edge and the O K edge, the spectra are also consistent with those of the LTO powder baseline (Figure S1 (e)).

The obtained LTO thin films were then electrochemically lithiated in coin cells using a commercial LP57 electrolyte with a

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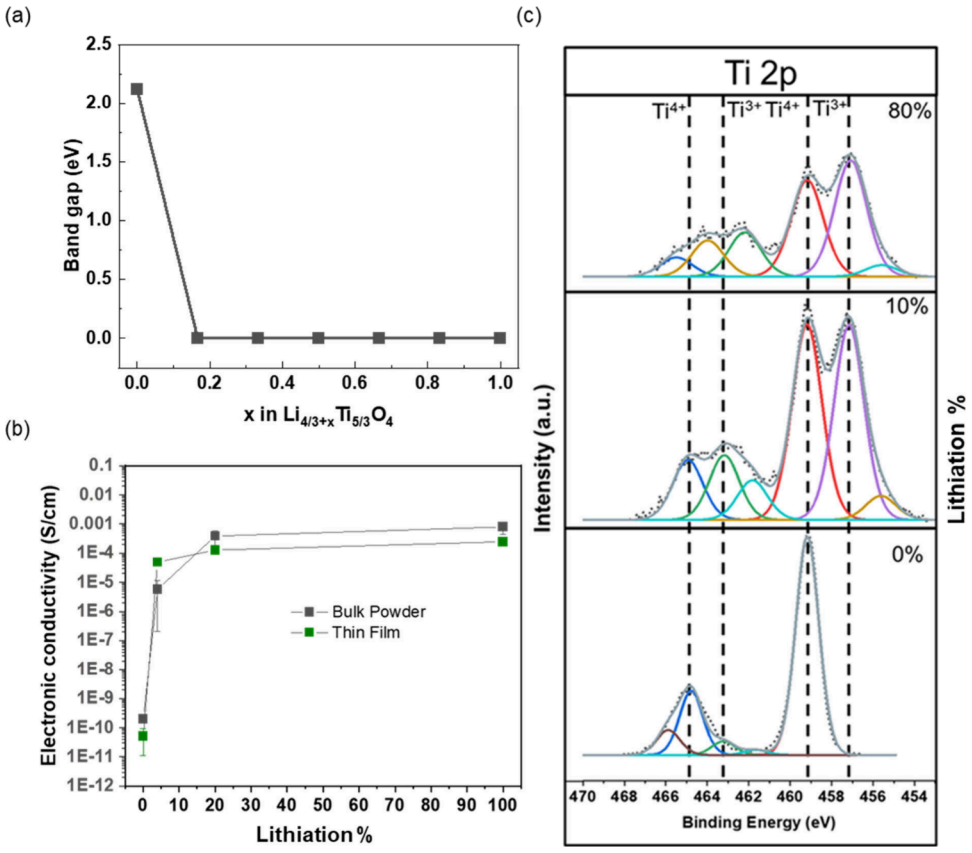

Figure 3. (a) Bandgap profile of $Li_{4/3+x}Ti_{5/3}O_4$ as a function of various amounts of lithium. (b) Electrical conductivity of LTO for various percentages of lithiation. (c) Ti 2p XPS spectra for various percentages of lithiation.

Li metal chip/foil as the counter electrode. For 100% lithiation, the thin film was lithiated to 1 V cutoff vs Li/Li^+. For 4% and 20% lithiation, a capacity cutoff based on the total capacity of 100% lithiation was used, as shown in Figure 2 (a). The plateau region in the voltage profile indicates the coexistence of the two-phase region of LTO upon lithiation, which has been widely studied and reported.[41−43] The lithiated thin films were disassembled from coin cells and washed in DMC to remove the residue electrolytes for further characterization. The optical images of the washed thin films show a color change from rose color for pristine LTO to green color for 100% lithiation, showing electrochromic behavior[44] (Figure 2 (a)).

The washed samples were then characterized using Raman spectroscopy with an airtight sample holder (Figure 2 (b)). Based on factor group analysis, there are five Raman peaks for pristine LTO, out of which are the three major Raman peaks of pristine LTO: F_{2g1} peak around 235 cm^{-1} which corresponds to bending vibrations of O−Ti−O bonds; E_g peak around 426 cm^{-1} which corresponds to asymmetric stretching of Li−O vibrations in LiO_4 tetrahedron; and A_{1g} peak around 672 cm^{-1} which corresponds to Ti−O vibration in TiO_6 octahedron.[45] The remaining two F_{2g} peaks (F_{2g2}, F_{2g3}) appear at approximately 270 cm^{-1} and in the 350 cm^{-1} region.[46] Beyond these five fundamental Raman-active peaks, pristine LTO spectra also exhibit what are commonly referred to as "surplus bands" and "satellite surplus bands".[46] The surplus bands appear notably at approximately 520 cm^{-1} and 310 cm^{-1}. However, they are generally indistinguishable at room temperature where our measurements are carried out. These surplus features are not predicted by theoretical calculations based on ideal crystal structures but are consistently observed in experimental measurements. These surplus bands arise from structural distortions and lattice defects present in real LTO samples. The satellite surplus bands often exist as the shoulders of the major Raman peaks such as at 260 cm^{-1} (shoulder to major F_{2g} peak), at 400 cm^{-1}(shoulder to E_g peak), and at 750 cm^{-1} (shoulder to A_{1g} peak).[46] For 4% lithiation, there is a slight red shift of the O−Ti−O vibration corresponding to a change in bond length due to the transformation of Ti^{4+}−O to Ti^{3+}−O. With further lithiation, for 20% lithiation, A_{1g} and E_g peaks have a lower intensity, whereas intensity of the F_{2g} peak increases, indicating that asymmetric stretching of the Li−O bond and symmetric stretching of the Ti−O bond become less pronounced. For a fully lithiated state or 100% lithiation, E_g and A_{1g} peaks are absent, and only the F_{2g} peak exists. The absence of the E_g peak indicates Li in tetrahedral positions moving to octahedral positions and forming the $Li_7Ti_5O_{12}$ phase.[47] Pasquini et al.[48] established that the Raman spectra can effectively track the electronic transition, with peak broadening serving as a direct indicator of the presence of mixed oxidation states in the crystal structure. The additional d-electron in Ti^{3+} modifies the force constants in the Ti−O bonds, creating heterogeneity in vibrational frequencies that manifests as peak broadening[49] of the F_{2g} mode.

Lithium Concentration Dependent Electronic Properties of LTO

DFT was applied to explain the phases formed during the lithium insertion into $Li_4Ti_5O_{12}$. For determining the density of states (DoS) for $Li_4Ti_5O_{12}$ (LTO) and $Li_7Ti_5O_{12}$ (lithiated LTO), a $Li_8Ti_{10}O_{24}$ 1 × 1 × 2 supercell was constructed as a

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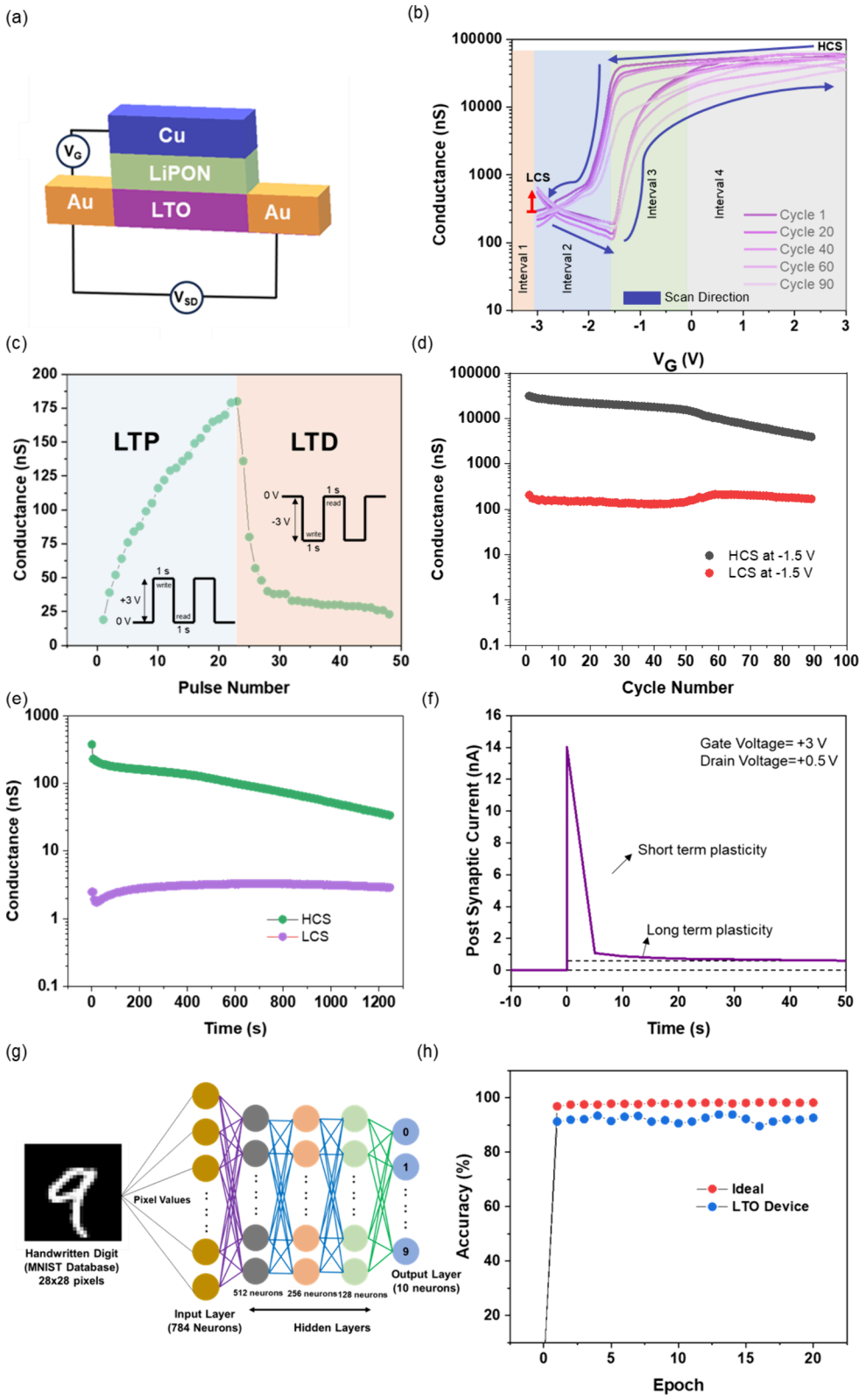

Figure 4. (a) Schematic of LTO Li-ion gated transistor. (b) Transfer characteristics of LTO Li-ion gated transistor for 90 cycles. (c) First cycle of long-term potentiation (LTP) and long-term depression (LTD) in the LTO Li-ion gated transistor. (d) Endurance test of the LTO Li-ion gated transistor done at a gate voltage of −1.5 V. (e) Retention test of the LTO Li-ion gated transistor. (f) EPSC response for a gate pulse of +3 V. (g) Schematic illustration of the deep neural network (DNN) for handwritten digit recognition. (h) Recognition accuracy as a function of training epoch for handwritten digit recognition.

pristine state (Figure S2 (a)) and $Li_{14}Ti_{10}O_{24}$ supercell was used as the fully lithiated state (Figure S2 (b)). The pristine spinel structure ($Li_4Ti_5O_{12}$) belongs to the $Fd\bar{3}m$ space group where Li occupies 8a sites and Li or Ti occupies 16d sites. The O in 32e

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sites is tetrahedrally coordinated to 8a sites and octahedrally coordinated to 16d sites. In this spinel structure, Li for every five Ti ions is occupied in 16d sites. During lithiation, Li ions in the 8a sites (yellow) and intercalated Li ions migrate to the 16c sites (cyan) to form the $Li_7Ti_5O_{12}$ Rocksalt phase. There is an absence of Li 8a sites in $Li_7Ti_5O_{12}$. The bandgap of fully relaxed LTO and its lithiated form were calculated using the GGA functional. The band gap of the pristine $Li_8Ti_{10}O_{24}$ (Figure 3 (a)) was found to be 2.1 eV, which shows that the pristine $Li_8Ti_{10}O_{24}$ is an insulator. The DFT calculation using the GGA functional underestimates the bandgap because it cannot describe the electron−electron correlation exchange interaction.[42,50] Upon addition of lithium atoms into the supercell, the bandgap was reduced to 0, indicating that the addition of Li makes LTO an electronic conductor. The DoS analysis in Figure S2 (c) further verified this trend, showing the DoS plot of the pristine LTO. The Fermi energy lies in the conduction band after adding 6 Li atoms in the supercell, indicating the metallic behavior for lithiated LTO (Figure S2 (d)). Our previous work has shown that the formation of intermediate phases is energetically not favorable, and the lithiation of LTO proceeds via the formation of a two-phase reaction (coexistence of $Li_4Ti_5O_{12}$ and $Li_7Ti_5O_{12}$ phases) rather than a solid solution reaction.[42]

The out-of-plane electronic conductivities of pristine LTO, 4% lithiation, 20% lithiation, and 100% lithiation thin films were then measured using DC polarization with the two-probe setup, as shown in Figure S3 (a) and (b). Additionally, pristine LTO powder was lithiated to 4% lithiation, 20% lithiation, and 100% lithiation in the split cell setup, as shown in Figure S4 (a), and its corresponding voltage profile for lithiation is shown in Figure S4 (b). The electronic conductivity of the powder samples was measured using the same split cell for baseline comparison to the thin film samples. The thin film and powder samples show six orders of jump in electronic conductivity, and the electronic conductivity values plateau after 20% lithiation (Figure 3 (b)). In batteries or other energy devices, full utilization of the active material is required to achieve the highest level of energy generation, conversion, or storage. However, our findings indicate that the highest possible switching can be observed, even with partial utilization of the active material. From our previous works on LTO[42] and LLTO,[21] we can infer that the plateauing of the electronic conductivity is a result of a "filament-like" lithiation of LTO. The EIS was done to understand the impedance evolution on pristine, 4% lithiation, and 100% lithiation thin films (Figure S3 (c)). The EIS spectra were modeled using two distinct equivalent circuits, as shown in Figure S3, with separate configurations required for pristine and lithiated LTO samples. The pristine LTO required a more complex circuit incorporating a Warburg element (W3) and an additional constant phase element (Q3), which were not necessary for modeling the lithiated samples. In the pristine LTO, the R2−Q2 parallel combination and the additional CPE (Q3) represent the combined contributions from grain boundaries and the electrode−electrolyte interfaces (LTO−Pt and LTO−Cu). The Warburg element (W3) characterizes the solid-state diffusion of Li+ ions through the bulk material, which manifests as the rate-limiting process in the pristine phase. Upon lithiation and formation of $Li_7Ti_5O_{12}$, two significant changes occur in the impedance response: (1) the Warburg element disappears, indicating that solid-state diffusion is no longer the rate-limiting step, and (2) the additional CPE (Q3) is eliminated while R2 decreases by approximately 4 orders of magnitude from 9.123 MΩ for pristine LTO to 2.7×10^{-4} MΩ for 100% lithiated LTO. The fitted parameters for the EIS measurement are shown in Table S2. These dramatic changes reflect the fundamental transformation in electronic structure during lithiation, where electron hopping pathways are created that substantially enhance both electronic and ionic conductivity throughout the material's microstructure, effectively homogenizing the previously distinct grain boundary and interface contributions. The Bode plot of LTO at different lithiation states reveals complementary information to the Nyquist plot (Figure S3 (d)). The pristine LTO exhibits high impedance ($\log|Z| \approx 7\ \Omega$) with a characteristic linearly decreasing slope at low frequencies indicative of diffusion-limited processes.[51] Upon lithiation, both 4% and 100% lithiated samples show dramatically reduced impedance (3.6 and 2.4 Ω, respectively) with relatively flat magnitude responses until approximately 10^3 Hz. The plateau regions in Bode plots indicate minimal diffusion contributions and are mostly capacitative.[52] This directly correlates with the progressive reduction of Ti^{4+} to Ti^{3+} during lithiation, creating percolation pathways for electronic conduction, while simultaneously eliminating the solid-state diffusion limitations that dominate in pristine LTO. The frequency-domain analysis thus provides clear evidence of how lithiation transforms $Li_4Ti_5O_{12}$ from an electronically insulating, diffusion-limited material to a mixed electronic−ionic conductor.

The XPS was acquired to understand the evolution of the oxidation state of Ti upon lithiation (Figure 3 (c)). For the pristine state or 0% lithiation, the Ti 2p spectrum is dominated by the two Ti^{4+} peaks, namely, Ti^{4+} $2p_{3/2}$ and Ti^{4+} $2p_{1/2}$, occurring at 459 and 465 eV, respectively. It confirms the +4 oxidation state of Ti in $Li_4Ti_5O_{12}$. Upon 10% lithiation, in addition to two Ti^{4+} peaks, there is an emergence of two Ti^{3+} peaks, namely, Ti^{3+} $2p_{3/2}$ and Ti^{3+} $2p_{1/2}$, occurring at 457 and 463 eV, respectively.[53] It indicates the coexistence of Ti^{4+} and Ti^{3+} oxidation states in the lithiated LTO. The Ti^{4+} has no electrons in three t_{2g} orbitals (d_{xy}, d_{yz}, d_{xz}) and two e_g orbitals (d_{x2-y2}, d_{z2}), whereas in the case of Ti^{3+}, there is one electron in the t_{2g} orbital which can act as a free electron for electrical conduction. Upon 80% lithiation, the ratio between Ti^{3+} and Ti^{4+} has notably increased, indicating that more $Li_4Ti_5O_{12}$ is being transformed to $Li_7Ti_5O_{12}$.

Device Characterization and Resistive Switching Mechanism

A resistive switching (RS) device was fabricated to verify the resistive switching property of the LTO upon lithiation. This Li-ion gated transistor is a three-terminal device with LTO as the channel layer, Au as the source and drain terminals, LiPON as the Li-ion source and ion conductor, and Cu as the gate terminal, as shown in Figure 4 (a). Figure S5 (a) shows the optical images of eight devices fabricated on a 1 cm × 1 cm alumina substrate, and Figure S5 (b) shows magnified SEM image of the surfaces of the four devices. From PFIB-SEM data in Figure S5 (c) and (d), we can see the cross section of one device, highlighting each layer in the device, namely, LTO (~80 nm), LiPON (~635 nm), and Cu (~150 nm). The gap between the source and drain terminals is 50 μm, which is the width of the LTO channel layer for each device. A small constant DC voltage (V_{DS}) is applied across the source and drain terminals to track the change in the measured current in the LTO channel layer. The voltage sweep applied across the gate and source/drain terminals (V_G) causes an ion gating effect that moves Li ions in LiPON into the LTO channel and out of the LTO channel based on the polarity of the

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voltage sweep. When the LiPON is deposited on LTO, the LTO region in contact with LiPON gets partially lithiated due to the chemical potential difference between LiPON and LTO, which drives Li from LiPON to LTO, thus reducing the oxidation state of Ti from 4^+ to 3^+. This phenomenon was previously observed in our work on the LNMO−LiPON interface.[54] This leads to the formation of a partially lithiated interface to begin with; this state is denoted as the low conductance state (LCS), and this region is labeled as Interval 1 (Figure 4 (b)). For the transfer characteristics of the device for Cycle 1, when a negative gate voltage sweep (V_G) commencing at −3 V is applied, the conductance reduces until −1.5 V, which is labeled Interval 2. This is caused by the migration of Li from the partially lithiated LTO channel into LiPON. Upon a further gate voltage sweep toward the positive bias until +3 V, there is an increase in conductance in the LTO channel and plateaus after +1 V, which are labeled as Interval 3 (−1.5 to 0 V) and Interval 4 (0 V to +3 V). The conductance state at +3 V is denoted as the high conductance state (HCS). Upon the voltage sweep in the opposite direction, the conductance does not change until −1.5 V, after which there is a steady decrease in conductance until −3 V caused by lithium moving out of the channel into LiPON. At the end of each cycle, the conductance state drops below the LCS (low conductance state). When the next cycle begins, the conductance returns to the LCS level (as shown by the red arrow). This behavior occurs because lithium ions from the LiPON diffuse into the Li-deficient LTO at the cycle's end. The constant DC voltage applied across source and drain terminals is 500 mV, and the gate voltage sweep rate is 90 mV/s. There is a clear hysteresis in the forward and backward sweep of the gate voltage, possibly due to the Li insertion and Li deinsertion process. The device has been run for 90 cycles; beyond 40 cycles, the plateau region is changed into a slopey region, and hysteresis is lowered. Figure S6a shows the transfer characteristics of the device as a function of both the source drain current (I_{DS}) and gate leakage current (I_{GS}) vs gate voltage over 90 cycles. The low I_{GS} relative to I_{DS} in this device provides two critical benefits: it minimizes power consumption through the gate electrode, thus improving energy efficiency, and indicates reduced faradaic reactions at the gate/electrolyte interface in the operation window showing enhanced electrochemical stability. Figure S6(b) shows the transfer characteristics of four tested devices, and Table S3 shows the statistical data of these four devices. In terms of variability across devices, based on the coefficient of variation, the most variation was observed for LCS and least for threshold voltage.

We have demonstrated the transfer characteristics of the device using varying source−drain DC voltages with a constant gate voltage sweep rate of 90 mV/s (Figure S7a) and varying gate voltage sweep rate with a constant source−drain voltage of 500 mV (Figure S7 (b)). As seen in Figure S7 (a), a minimum source−drain voltage (∼100 mV) is required for a specific size and geometry of the device, below which the transfer characteristics show several conductance fluctuations. Figure S7 (b) shows that as the gate voltage sweep rate increases, an increased hysteresis loop area indicates an enhanced memory effect. The hysteresis in the gate voltage sweep rate possibly arises from three key mechanisms: diffusion-limited ion transport in $Li_4Ti_5O_{12}$ vs capacitance dominating in $Li_7Ti_5O_{12}$ previously described by Nyquist and Bode plots (Figure S3 (c) and (d)) which creates concentration gradients during higher rates; charge transfer resistance at the LTO/LiPON interface;[40] and space charge layer (SCL) capacitance effects at solid−solid interfaces.[55] Despite the correlation between faster sweep rates and increased hysteresis, we deliberately selected 90 mV/s—the slowest tested sweep rate for all subsequent device measurements—to ensure that Li-ion intercalation/deintercalation is still possible while maintaining reasonable measurement timeframes and signal quality without introducing kinetic artifacts.

To further confirm that hysteresis is caused by the Li insertion and deinsertion process, a control device with silicon nitride (Si_3N_4) replacing LiPON was fabricated, as shown in Figure S8 (a) and (b). The Si_3N_4 was chosen to avoid any extra Li source apart from lithium in LTO. DC polarization was performed for the Si_3N_4 layer (Figure S8 (c)) to determine the electrical conductivity, and it was compared with the LiPON layer (Figure S8 (d)). The electrical conductivities of LiPON and Si_3N_4 are 4.1×10^{-12} S/cm and 5.6×10^{-10} S/cm, respectively, indicating that the deposited Si_3N_4 layer is an electrical insulator even though the deposited LiPON layer has lower electrical conductivity by 2 orders of magnitude. The fabricated device was tested by using the same measurement protocol as the device with LiPON. Figure S8 shows the transfer characteristics of the device for one cycle commencing at −3 V with a gate voltage sweep rate of 90 mV/s and a constant DC voltage of 500 mV. Unlike in the case of the LiPON-based device where LiPON acts as the extra Li source, in the Si_3N_4-based device, there is no hysteresis; however, a large jump in conductance was still observed. It confirms that mobile ions such as Li^+ are responsible for the hysteresis, which is absent in Si_3N_4 as it has very strong Si−N covalent bonds, leading to extremely low ion mobility[56] and no ion insertion into the channel layer. The sharp conductance transition likely originates from the bias-induced formation of heterogeneous lithium distribution in the LTO channel, where coexisting Li-rich and Li-poor domains establish an electronically percolating network, a phenomenon previously documented in mixed ionic−electronic conductors.[21,31,45]

Long-term potentiation (LTP) and long-term depression (LTD) measurements characterize how the synaptic strength, represented by channel conductance, responds to external gate voltage pulses. These tests can demonstrate the device's ability to emulate biological synaptic plasticity by showing persistent increases (LTP) or decreases (LTD) in conductance following specific stimulation protocols. The parameters obtained through the LTP−LTD test, such as the extent of nonlinearity, maximum and minimum conductance ratio (G_{max}/G_{min}), and asymmetric ratio (AR), are crucial for training and prediction tasks when implementing neuromorphic hardware for neural networks.[57] For LTP, we applied sequential positive voltage pulses (+3 V amplitude, 1 s duration—write mode) alternating with resting periods (0 V, 1 s duration—read mode)—pulse scheme in the Figure 4 (c) inset. This controlled pulse−rest pattern progressively enhanced the channel conductance from 19 to 180 nS over 23 pulses. For LTD, we applied sequential negative voltage pulses (−3 V amplitude, 1 s duration—write mode) alternating with similar resting periods (0 V, 1 s duration—read mode)—pulse scheme in the Figure 4 (c) inset. This pattern gradually attenuated the channel conductance back to 23 nS over 25 pulses. Throughout the experiment, conductance values were extracted from current measurements taken during both write and read operations, using a fixed source−drain bias voltage (V_{DS}) of 500 mV. The data points plotted in Figure 4 (c) represent conductance calculated from the current obtained during the "write mode" from the LTO channel for each pulse. Figure S9 (a) shows the fitting results of this LTP−LTD data to

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obtain the nonlinearity factor, G_{max}/G_{min}, and AR. The equations for LTP and LTD fitting are defined in Supplementary Note 2. We also defined a shape factor β for LTD to improve the fit for the LTD profile. We extracted parameters for our synaptic plasticity equations using nonlinear least-squares optimization via SciPy's curve_fit function. After preprocessing conductance data to determine g_min_val and g_max_val, we fitted the LTP equation using an initial v_p guess of 0.5 (bounded between 0.01 and 10.0) to minimize the difference between experimental and model-predicted conductance values. For LTD, we performed a two-parameter fit for both v_d and β, with initial guesses of 0.5 and 1.0, respectively, and bounds of ([0.01, 0.1], [10.0, 5.0]). The fitting quality was validated using R^2 values calculated with sklearn's r2_score function and visual inspection of fitted curves against experimental data. The β parameter was specifically introduced to capture asymmetric depression behavior via the normalized pulse representation ($p/\max(p_{ltd}) - 1$) and the sign function. Additionally, we calculated the Asymmetric Ratio (AR) as the ratio between the conductance change during potentiation ($\Delta G\_LTP = \max(ltp_{conductance}) - \min(ltp_{conductance})$) and the conductance change during depression ($\Delta G\_LTD = \max(ltd_{conductance}) - \min(ltd_{conductance})$), which provides a quantitative measure of the asymmetry between potentiation and depression behaviors in our synaptic device. The code for running the fitting and the simulation can be found in Supporting Information 2, and we used Sandia National Lab's CrossSim platform for the simulation.[58] These extracted parameters provide insights into device nonlinearity and determine how well our devices can implement synaptic weight updates in neuromorphic applications. For our comprehensive device characterization, we conducted both endurance and retention tests on the LTO-based Li-ion transistor (Figure 4 (d) and (e)). For the endurance test, we specifically targeted the −1.5 V gate voltage point where the transfer characteristics exhibited the maximum conductance gap between states, measuring both HCS and LCS at this voltage across 90 complete cycles. For the retention testing protocol, we employed a systematic approach wherein the device was first swept from −3 V to +3 V to achieve the HCS and then monitored at 5 s intervals with a constant DC V_{DS} of 500 mV; similarly, for LCS, the device was swept from −3 V to −3 V and monitored under identical conditions. Our endurance testing revealed excellent cycling stability, with the HCS diminishing from 30,000 nS to 4,000 nS—representing about an order of magnitude in decay—while the LCS exhibited remarkable stability by maintaining consistent conductance around 170−200 nS throughout all cycles. The initial switch ratio (HCS/LCS) was 153, and after 90 cycles, it was 23. The retention characteristics, measured over a 20 min period (1200 s), showed that the HCS exhibited a gradual decay from approximately 400 nS to 30 nS following a logarithmic relaxation pattern typical of charge storage devices, whereas the LCS (purple) demonstrated exceptional stability by starting at around 2 nS, briefly rising to approximately 3 nS, and then maintaining this level for the remainder of the test, resulting in a clear conductance window of approximately 10 between states even after 1200 s—sufficient for reliable state differentiation in practical applications. An excitatory postsynaptic current (EPSC) measurement was done using a +3 V gate voltage pulse at a pulse interval of 1 s and V_{DS} = 0.5 V. The post synaptic current is the I_{DS} and summarized in Figure 4 (f). From the peak current (I_{peak}) observed in the EPSC data, the energy consumed per synaptic event can be calculated using the formula $E_{spike} = I_{peak} \times t_w \times V_{DS}$, where t_w represents the pulse width.[59] Applying this equation to the device stimulated with a +3 V gate pulse for 1 s and operating at V_{DS} = 0.5 V yields E_{spike} = 7 nJ, which falls within the range of many reported artificial synaptic devices in current literature.[60,61] This energy consumption metric is particularly significant when evaluating neuromorphic computing efficiency, as biological neuronal spikes operate at remarkably lower energy scales—typically in the femtojoule (fJ) range.[28] The 3 orders of magnitude difference between our device (nJ) and biological systems (fJ) highlights a critical area for future optimization. Apart from transfer characteristics, we performed output characteristics on the device as shown in Figure S10, sweeping V_{DS} from 100 to 1000 mV while maintaining constant gate voltages of 0, 1, 2, and 3 V. The resulting output characteristics reveal distinct transport regimes characteristic of this lithium-ion transistor. In the low-voltage region (0−400 mV), all curves exhibit clearly linear behavior where I_{DS} increases proportionally with V_{DS}, indicating ohmic conduction through the LTO channel. A pronounced transition occurs at approximately 500 mV, where the slope decreases markedly, leading to an unusual plateau region (500−800 mV) where current remains nearly constant or displays a slight negative differential resistance. Beyond 800 mV, all curves demonstrate a secondary rise in I_{DS} with increasing V_{DS}, suggesting that complete channel saturation occurs beyond the measured range of 1000 mV.

From the LTP−LTD fitting, the following parameters were obtained: the asymmetric ratio (AR) was 1.425, the LTP nonlinearity factor (v_p) was 1.103, the LTD nonlinearity factor (v_d) was 3.529, G_{max}/G_{min} was 7.83, and finally the shape factor (β) for LTD was 0.374. These parameters along with the device noise data were used to train a deep neural network (DNN) for recognizing handwritten digits from the MNIST database. The DNN consists of 784 neurons as the input layer, three hidden layers, each composed of 512 neurons, 256 neurons, 128 neurons, and the final output layer consisting of 10 neurons for each digit output (Figure 4 (g)). The summary of the recognition accuracy is shown in Figure 4 (h). For the ideal case without considering any device-related parameters, the average accuracy for 20 training epochs is 97.86%, whereas for the LTO device-specific case, the average accuracy for 20 training epochs is 92.03%. The LTP and LTD tests were then performed for subsequent cycles and shown as a function of read current and pulse number (Figure S9 (b)) and a function of write current and pulse number (Figure S9 (c)). For each cycle, there were 25 pulses for LTP and LTD, and it can be noticed that for every cycle, the maximum conductance (G_{max}) achieved during LTP increased. While the precise mechanism underlying this phenomenon remains under investigation, we hypothesize that the progressive conductance enhancement stems from cycle-dependent lithium accumulation in the channel in the form of the conductive $Li_7Ti_5O_{12}$ phase. This accumulation is likely due to kinetic limitations during the high pulse rates during the LTP and LTD tests. These residual lithium-rich domains can coalesce into more significant conductive regions, consequently increasing the overall channel conductance. A systematic investigation of the underlying mechanism could be achieved through extended LTP−LTD testing protocols, incorporating prolonged pulse durations and rest intervals to better elucidate the kinetics of lithium accumulation and conductive domain formation. The device's nonvolatile behavior is as important as the jump in conductance state during potentiation and depression for neuromorphic computing architecture.

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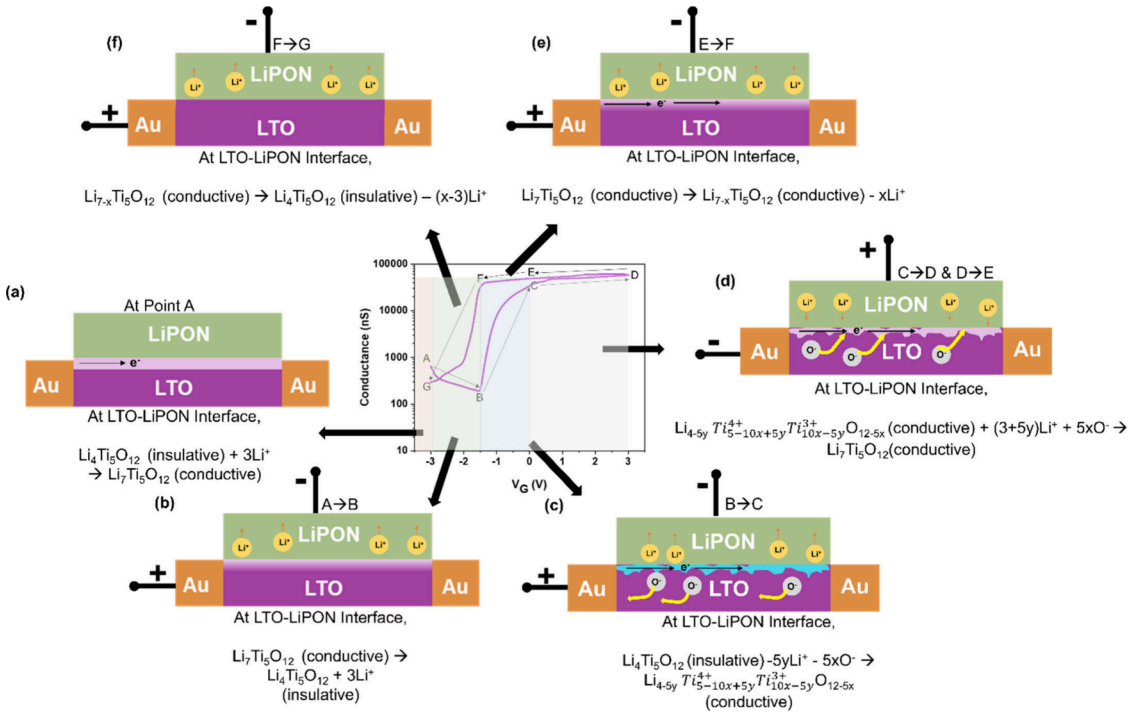

Figure 5. (a) Overlithiated LTO at the interface at point A. (b) For the A to B path, Li transport is out of the channel. (c) For the B to C path, further Li transport happens away from the channel, accompanied by the formation of oxygen vacancies. (d) For the C to D and D to E regions, Li transport is toward the channel, accompanied by disappearance of oxygen vacancies. (e) For the E to F path, Li transport is away from the channel. (f) For the F to G path, Li transport is further away from the channel.

An understanding of various transport mechanisms is crucial for optimizing device performance. Figure 5 illustrates our hypothesis summarizing possible transport processes in the Li-ion gated transistor. At the beginning of the operation of the device (at point A), LTO's interface region with LiPON is overlithiated, exhibiting higher conductance than expected for the LTO channel. This phenomenon is either caused by the higher chemical potential of Li in LiPON that drives Li into the LTO[18] or it could be due to the lithiation of the LTO's interface during the deposition of LiPON[31,62] (Figure 5 (a)). When a negative bias is applied initially from point A to B, the Li ion migrates out of the overlithiated interface of the LTO channel, consequently reducing the conductance as described in Figure 5 (b). The minimum conductance is reached when all of the excess Li is moved out of the interface of the LTO channel with LiPON (point B). Notably, further lithium extraction necessitates the formation of oxygen vacancies at the interface. This requirement stems from the fact that when all of the excess Li is extracted, LTO exists in the $Li_4Ti_5O_{12}$ phase in which the oxidation state of Ti is 4+. Further removal of Li makes the oxidation state of Ti greater than 4+. The oxidation state cannot exceed 4+ since its electronic configuration $[Ar]3d^24s^2$ permits removal of only valence electrons to achieve a stable [Ar] configuration. Further oxidation would require removing an electron from the complete [Ar] core, which is energetically unfavorable. So, oxygen vacancies have to be generated for the charge balance. Therefore, oxygen vacancies are also formed for the path between points B and C, along with some lithium extraction, as shown in Figure 5 (c). The resulting lithium–oxygen vacant LTO is conductive due to the possibility of the formation of a Ti^{3+} valence state, which is why the conductance of the channel increases between points B and C. We have done DFT calculations on the same 1 × 1 × 2 supercell of $Li_8Ti_{10}O_{24}$ to understand the influence of oxygen vacancies on the electronic structure of LTO as shown in Figure S11. Figure S11(a) reveals a dramatic electronic transformation in $Li_4Ti_5O_{12}$ (LTO) upon introducing oxygen vacancies, where the substantial bandgap (~2.1 eV) completely collapses to near zero, converting LTO from an insulator to a material with metallic-like conductivity. This transformation occurs because oxygen vacancies can also create excess electrons that reduce Ti^{4+} to Ti^{3+}, introducing midgap states that facilitate electronic conduction, as confirmed by the density of states plot showing continuous states across the Fermi level (Figure S11 (b)). Interestingly, both pristine and oxygen-deficient LTOs converge to similar electronic structures at higher lithiation levels. For the path between C to D and D to E, the direction of Li-ion flow is reversed as shown in Figure 5 (d), and now Li flows into the channel. At the same time, the source is at a negative polarity, which means oxygen ions, which were migrated to create oxygen vacancies in the path between B and C, will be repelled and move toward the interface. This interface can form lithiated LTO. Further, for the path between E to F, the direction of Li-ion flow is once again reversed and now Li moves out of the channel as shown in Figure 5 (e). In this path, the interface is still conductive as most of the interface is still the lithiated LTO. As discussed in Figure 3 (b), the lithiation process in LTO is plateau-like after ~20% lithiation below which there is an abrupt decrease in electrical conductivity, and we can see a similar process happen in the path between F and G (Figure 5 (f)) where further Li removal leads to an abrupt decrease in conductance until at point G where it is supposed to form the pristine LTO which is insulative. Upon closer observation on the proposed mechanism described here, it can be noticed that the mechanisms of the path from A to D is not the same as D to G, and we believe that this difference could be another cause of the

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hysteresis which is affected by the transport properties of oxygen vacancies as well as Li-ion flow.

CONCLUSION

Our study comprehensively investigated $Li_4Ti_5O_{12}$ for resistive switching applications, focusing on the electronic and ionic transport mechanisms at both material and device levels. Upon electrochemical lithiation, LTO demonstrates systematic phase transformation from $Li_4Ti_5O_{12}$ to $Li_7Ti_5O_{12}$, as evidenced by Raman spectroscopy showing the evolution of characteristic F_{2g}, E_g, and A_{1g} peaks. The DFT calculations reveal a critical transition from insulating to conducting behavior upon lithiation, with the bandgap decreasing from 2.1 to 0 eV, supported by experimental measurements in thin film and powder form, showing a remarkable six-order magnitude increase in electronic conductivity. The fabricated three-terminal Li-ion gated transistor, comprising LTO as the channel layer, Au as the source and drain terminals, LiPON as the ion conductor, and Cu as the gate terminal, demonstrates resistive switching characteristics with distinct high and low conductance states. The device exhibits synaptic plasticity-like behavior with LTP and LTD characteristics, achieving an asymmetric ratio of 1.425, LTP nonlinearity factor of 1.103, LTD nonlinearity factor of 3.529, and a maximum/minimum conductance ratio of 7.83. When these device characteristics were implemented in a deep neural network (DNN) architecture for handwritten digit recognition (from the MNIST Database), the device achieved an accuracy of 92.03% over 20 training epochs, compared to 97.86% for ideal conditions. The resistive switching mechanism in the device is elucidated through a detailed analysis of the LTO−LiPON interface, revealing a complex interplay between Li-ion transport and oxygen vacancy formation. Initial over-lithiation at the interface, caused by chemical potential differences, leads to enhanced conductance, while subsequent voltage-controlled Li migration and oxygen vacancy formation govern the device's switching behavior. This understanding of the transport mechanisms provides crucial insights into optimizing ionic−electronic devices for neuromorphic computing applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaenm.5c00459.

Details of the experimental methods (PDF)

Python code for MNIST simulation employing the deep neural network (DNN) model (PDF)

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Notes

The authors declare no competing financial interest.

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